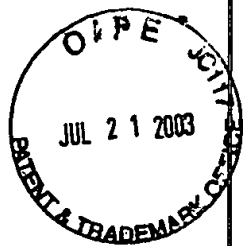


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



Applicant(s): Jack H. Yuan et al.
Assignee: SanDisk Corporation
Title: Scalable Self-Aligned Dual Floating Gate Memory Cell Array and
Methods of Forming the Array
Serial No.: 09/925,102 Filing Date: August 8, 2001
Examiner: Unknown Group Art Unit: 2185
Docket No.: M-11822 US Conf. No.: 3186

COPY
San Francisco, California
July 22, 2002

COMMISSIONER FOR PATENTS
Washington, D. C. 20231

**INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR § 1.97(b)**

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying form PTO-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.


Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

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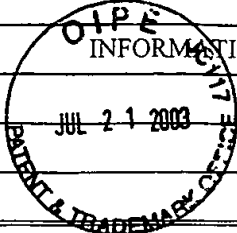
Respectfully submitted,

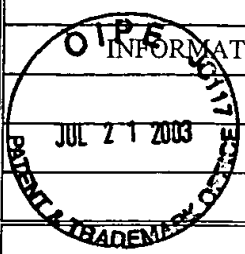

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U.S. Department of Commerce, Patent and Trademark Office					Atty Docket No.		Serial No.	
					M-11822 US		09/925,102	
					Applicant(s)			
(Use several sheets if necessary)					Jack H. Yuan et al.			
					Filing Date		Group	
					August 8, 2001		2185	
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	5,043,940	Aug. 27, 1991	Harari				
	AB	5,070,032	Dec. 3, 1991	Yuan et al.				
	AC	5,095,344	Mar. 10, 1992	Harari				
	AD	5,172,338	Dec. 15, 1992	Mehrotra et al.				
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	AK	6,103,573	Aug. 15, 2000	Harari et al.				
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	AL	Aritome, Seiichi, "Advanced Flash Memory Technology and Trends for File Storage Application," IEDM Technical Digest, International Electronic Devices Meeting, IEEE, San Francisco, California, December 10-13, 2000, pp 33.1.1-33.1.4.						
	AM	Takeuchi, Y., et al., "A Self-Aligned STI Process Integration for Low Cost and Highly Reliable 1Gbit Flash Memories," 1998 Symposium on VLSI Technology; Digest of Technical Papers, IEEE, Honolulu, Hawaii, June 9-11, 1998, pp. 102-103.						
	AN	Lee, Jae-Duk, et al., "Effects of Parasitic Capacitance on NAND Flash Memory Cell Operation," Non-Volatile Semiconductor Memory Workshop, IEEE, Monterey, California, August 12-16, 2001, pp. 90-92.						
	AO	Chan, et al., "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device," <i>IEEE Electron Device Letters</i> , Vol. EDL-8, No. 3, March 1987, pp. 93-95.						
Examiner			Date Considered					
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>								

U.S. Department of Commerce, Patent and Trademark Office						Atty Docket No.		Serial No.	
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U.S. Patent Documents									
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
	AP	6,151,248	Nov. 21, 2000	Harari et al.					
	AQ	6,222,762	Apr. 24, 2001	Guterman et al.					
Foreign Patent Documents									
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		Document	Date	Country	Class	Subclass	Yes	No	
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)									
	AR	Nozaki et al., "A 1-Mb EEPROM with MONOS Memory Cell for Semiconductor Disk Application," <i>IEEE Journal of Solid State Circuits</i> , Vol. 26, No. 4, April 1991, pp. 497-501.							
	AS	Eitan et al., "NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell," <i>IEEE Electron Device Letters</i> , Vol. 21, No. 11, November 2000, pp. 543-545.							
	AT	DiMaria et al., "Electrically-alterable read-only-memory using Si-rich SiO ₂ injectors and a floating polycrystalline silicon storage layer," <i>J. Appl. Phys.</i> 52(7), July 1981, pp. 4825-4842.							
	AU	Hori et al., "A MOSFET with Si-implanted Gate-SiO ₂ Insulator for Nonvolatile Memory Applications," <i>IEDM 92</i> , April 1992, pp. 469-472.							
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